TABLE 3-continued

	R[0:5]	G[0:5]	B[0:5]	REV
Dn + 3	001101	111111	001110	High
Dn + 4	001101	000000	001110	High

If the data as described in Table 2 and the mode control signal REV are input over the transmission line **42**, then the data receiver **38** reconstructs the data into the original data output from the interface **34** as described in Table 3, and outputs the reconstructed data to the D-ICs **32**. As described above, the data receiver **38** selectively inverts the 18 bit video data from the data transmitter **36** in response to the mode control signal REV, thereby being reconstructed into the original video data **R0** to **B5**.

FIG. **10** shows another embodiment of the data receiver **38** in FIG. **3**. In FIG. **10**, the data receiver **38** is configured similarly to the data transmitter **36** shown in FIG. **8**. Each exclusive OR gate EOX19 to EOX36 responds to the applied mode control signal REV to selectively invert the video data input over the transmission line **42**, and transfers the selectively inverted video data to the D-ICs **32**. The above-mentioned data receiver **38** may be integrated within the D-ICs **32**. An example of the D-ICs having such a configuration is disclosed in the Japanese Patent Laid-open Gazette No. Pyung 3-208090.

The above-mentioned embodiments of the present invention have been explained base on a liquid crystal display device employing a D-IC with a so-called single bank structure. In a liquid crystal display device having a double bank structure, 18 bit even-numbered video data and 18 bit odd-numbered video data are transmitted from the interface **34**. For such structure, the embodiment of the present invention can be implemented by transmitting the video data along twice the number of transmission lines and setting the critical bit number is then set to, for example, "18" in addition to the configuration as shown in FIG. **3** to FIG. **10**. This is because 36 bits of data are transmitted over the transmission line between the interface and the D-ICs in the liquid crystal display device.

Referring now to FIG. **11**, there is shown a computer system employing a data transmission apparatus according to another embodiment of the present invention. The computer system includes a data transmitter **36** and a data receiver **38** that are connected, in series, between a video card **62** within a computer main body **60** and an interface **34**, and a mode controller **40** for controlling transmission modes of the data transmitter **36** and the data receiver **38**. The video card **62** generates video data and a clock CLK. The video data includes red data (R0 to R5), green data (G0 to G5) and blue data (B09 to B5), each of which has 6 bit, for example. The data transmitter **36** is electrically connected to the data receiver **38** preferably by means of an FPC film **42**. The FPC film **42** includes 18 data bit lines, at least one of data clock line and a single mode line, or both. The data transmitter **36** selectively inverts 18 bit video data to be transmitted from the video card **62** to the data receiver **38** in accordance with a logic value of a mode control signal REV from the mode controller **40**. In a similar manner, the data receiver **38** selectively inverts the 18 bit video data R0 to B5 to be transmitted from the data transmitter **36** to the interface **34** in accordance with the logic value of the mode control signal REV from the mode controller **40**. Accordingly, an EMI at the video card **62** and the FPC film **42** can be minimized and a power consumption in the video card **62** can be reduced. Finally, the interface **34** supplies the video data reconstructed by the data receiver **38** to, for example, the liquid crystal display device and other suitable devices.

Referring to FIG. **12**, there is shown a computer system employing a data transmission apparatus according to still another embodiment of the present invention. The computer system includes a data transmitter **36** and a data receiver **38** that are connected, in series, between a video card **62** and D-ICs **32**, and a mode controller **40** for controlling transmission modes of the data transmitter **36** and the data receiver **38**. The data transmitter **36** is electrically connected to the data receiver **38** preferably by means of an FPC film **42**. The FPC film **42** includes 18 data bit lines, at least one of data clock line and a single mode line or both. The data transmitter **36** selectively inverts 18 bit video data to be transmitted from the video card **62** to the data receiver **38** in accordance with a logic value of a mode control signal REV from the mode controller **40**.

In response to the mode control signal REV generated at the mode controller **40**, the data transmitter **36** and the data receiver **38** selectively invert the video data to lower a frequency (or the number of transitions in the logic state) of the video data transmitted over the FPC film **42**. Accordingly, EMI at the video card **62** and the FPC film **42** can be restrained or minimized and power consumption in the video card **62** can be reduced.

As described above, in the data transmission apparatus and method according to the present invention, a data stream transmitted over a number of bit lines is inverted or not inverted according to the number of bit transitions in the data stream. For example, the bits of the data stream is inverted if the number of bit transitions exceeds a critical value, thereby lowering the number of transitions, that is, the frequency of the data stream. As a result, the data transmission apparatus and method of the present invention is capable of restraining or minimizing EMI at the transmission line as well as reducing power consumption at the data transmission side. Furthermore, in the liquid crystal display device, the computer interface device, and the computer system to which the data transmission according to the present invention is applied, EMI and power consumption at the video card and/or the interface can be reduced.

It will be apparent to those skilled in the art that various modifications and variation can be made in the data transmission apparatus and method of the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. A data transmission system comprising:

a mode controller receiving first data having a plurality of bits and outputting a first control signal in accordance with a number of data transitions of the plurality of bits of the data;

a data transmitter coupled to the mode controller and outputting second data corresponding to the first data in response to the first control signal from the mode controller; and

a data receiver coupled to the data transmitter and outputting third data corresponding to the second data in response to a second control signal corresponding to the first control signal.

2. The data transmission system according to claim **1**, wherein the first and second control signals are the same signal.

3. The data transmission system according to claim **1**, wherein the second data is an inverse of the first data depending on the first control signal.

4. The data transmission system according to claim 1, wherein the third data is an inverse of the second data depending on the second control signal.

5. The data transmission system according to claim 1, wherein the third data is the same as the first data.

6. The data transmission system according to claim 1, wherein the mode controller comprises:

transition detecting unit receiving the first data and detecting a transition in the plurality of bits of the first data;

a counter coupled to the transition detecting unit counting the number of transitions in the plurality of bits of the first data;

a comparator coupled to the counter comparing the number of transitions to a reference value; and

an output unit coupled to the comparator and outputting the first control signal.

7. The data transmission system according to claim 6, wherein the reference value is one of N/2, (N/2−1), and (N/2+1), where N is the number of bits of the first data.

8. The data transmission system according to claim 6, wherein the transition detecting unit comprises a plurality of transition detecting cells corresponding to the plurality of bits of the first data.

9. The data transmission system according to claim 8, wherein each of the transition detecting cell includes:

first flip-flop having a first output;

second flip-flop having a second output, the second flip-flop receiving the first output of the first flip-flop; and

a logic unit receiving the first and second outputs from the first and second flip-flops and outputting a third output, the third output containing information on a data transition of a corresponding bit of the plurality of the data bits of the first data.

10. The data transmission system according to claim 1, wherein the data transmitter comprises a control unit receiving the first data, an inverse of the first data, and the first control signal and outputting the second data, the second data being one of the inverse of the first data or the first data.

11. The data transmission system according to claim 1, wherein the data transmitter includes a logic unit receiving the first data and the first control signal and outputting the second data, the second data being one of the inverse of the first data or the first data.

12. The data transmission system according to claim 11, wherein the logic unit includes a plurality of exclusive OR gates.

13. The data transmission system according to claim 1, wherein the data receiver comprises a control unit receiving the second data, an inverse of the second data, and the second control signal and outputting the third data, the third data being one of the inverse of the second data or the second data.

14. The data transmission system according to claim 1, wherein the data receiver includes a logic unit receiving the second data and the second control signal and outputting the third data, the third data being one of the inverse of the second data or the second data.

15. The data transmission system according to claim 14, wherein the logic unit includes a plurality of exclusive OR gates.

16. A data transmission system for a computer comprising:

a main control unit including:

a video card outputting first data;

a mode controller receiving first data having a plurality of bits and outputting a first control signal in accordance with a number of data transitions of the plurality of bits of the data; and

a data transmitter coupled to the mode controller and outputting second data corresponding to the first data in response to the first control signal from the mode controller; and

a display unit coupled to the main control unit including:

a data receiver coupled to the data transmitter and outputting third data corresponding to the second data in response to a second control signal corresponding to the first control signal; and

data driver coupled to the data receiver and receiving the third data.

17. A data transmission system for a computer according to claim 16, further comprising an interface unit between the data receiver and the data driver.

18. A data transmission system for a computer according to claim 16, wherein the data receiver and the data driver are in one unit.

19. A liquid crystal display device having a data transmission system comprising:

a mode controller receiving first data having a plurality of bits and outputting a first control signal in accordance with a number of data transitions of the plurality of bits of the data;

a data transmitter coupled to the mode controller and

outputting second data corresponding to the first data in response to the first control signal from the mode controller; and

a data receiver coupled to the data transmitter and outputting third data corresponding to the second data in response to a second control signal corresponding to the first control signal.

20. The liquid crystal display device according to claim 19, wherein the first and second control signals are the same signal.

21. The liquid crystal display device according to claim 19, wherein the second data is an inverse of the first data depending on the first control signal.

22. The liquid crystal display device according to claim 19, wherein the third data is an inverse of the second data depending on the second control signal.

23. The liquid crystal display device according to claim 19, wherein the third data is the same as the first data.

24. The liquid crystal display device according to claim 19, wherein the mode controller comprises:

transition detecting unit receiving the first data and detecting a transition in the plurality of bits of the first data;

a counter coupled to the transition detecting unit counting the number of transitions in the plurality of bits of the first data;

a comparator coupled to the counter comparing the number of transitions to a reference value; and

an output unit coupled to the comparator and outputing the first control signal.

25. The liquid crystal display device according to claim 24, wherein the reference value is one of N/2, (N/2−1), and (N/2+1), where N is the number of bits of the first data.

26. The liquid crystal display device according to claim 24, wherein the transition detecting unit comprises a plurality of transition detecting cells corresponding to the plurality of bits of the first data.

27. The liquid crystal display device according to claim 26, wherein each of the transition detecting cell includes:

first flip-flop having a first output;

second flip-flop having a second output, the second flip-flop receiving the first output of the first flip-flop; and

a logic unit receiving the first and second outputs from the first and second flip-flops and outputting a third output, the third output containing information on a data transition of a corresponding bit of the plurality of the data bits of the first data.

28. The liquid crystal display device according to claim **19**, wherein the data transmitter comprises a control unit receiving the first data, an inverse of the first data, and the first control signal and outputting the second data, the second data being one of the inverse of the first data or the first data.

29. The liquid crystal display device according to claim **19**, wherein the data transmitter includes a logic unit receiving the first data and the first control signal and outputting the second data, the second data being one of the inverse of the first data or the first data.

30. The liquid crystal display device according to claim **29**, wherein the logic unit includes a plurality of exclusive OR gates.

31. The liquid crystal display device according to claim **19**, wherein the data receiver comprises a control unit receiving the second data, an inverse of the second data, and the second control signal and outputting the third data, the third data being one of the inverse of the second data or the second data.

32. The liquid crystal display device according to claim **19**, wherein the data receiver includes a logic unit receiving the second data and the second control signal and outputting the third data, the third data being one of the inverse of the second data or the second data.

33. The liquid crystal display device according to claim **32**, wherein the logic unit includes a plurality of exclusive OR gates.

34. A computer comprising:

a main control unit including:

a video card outputting first data;

a mode controller receiving first data having a plurality of bits and outputting a first control signal in accordance with a number of data transitions of the plurality of bits of the data; and

a data transmitter coupled to the mode controller and outputting second data corresponding to the first data in response to the first control signal from the mode controller; and

a display unit coupled to the main control unit including:

a data receiver coupled to the data transmitter and outputting third data corresponding to the second data in response to a second control signal corresponding to the first control signal; and

data driver coupled to the data receiver and receiving the third data.

35. A computer according to claim **34**, further comprising an interface unit between the data receiver and the data driver.

36. A computer according to claim **34**, wherein the data receiver and the data driver are in one unit.

37. A method of transmitting data comprising the steps of:

receiving first data having a plurality of bits and

outputting a first control signal in accordance with a number of data transitions of the plurality of bits of the data;

outputting second data corresponding to the first data in response to the first control signal; and

outputting third data corresponding to the second data in response to a second control signal corresponding to the first control signal.

38. A data transmission apparatus, comprising:

a mode controller for receiving a first data having a plurality of bits and a clock signal to detect a number of transitions of the first data corresponding to the clock signal and for generating a mode control signal having a logic value changing in accordance with the number of transitions;

a data transmitter, responsive to the mode control signal, for selectively inverting the first data and transmitting the inverted data; and

a data receiver, responsive to the mode control signal, for selectively inverting the selectively inverted data from the data transmitter to reconstruct the selectively inverted data into the first data.

39. A data transmission method comprising the steps of:

receiving a first data having a plurality of bits and a clock signal to detect a number of transitions in the first data corresponding to the clock signal and generating a mode control signal having a logic value changing in accordance with the number of transitions;

selectively inverting the first data in response to the mode control signal and transmitting the inverted data; and

selectively inverting the selectively inverted data in response to the mode control signal and reconstructing the inverted data into the first data.

40. A liquid crystal display device having a data driver for driving a liquid crystal panel, comprising:

a mode controller for receiving video data having a plurality of bits to detect a number of transitions between a first video data and a second video data and for generating a mode control signal having a logic value changing in accordance with the number of transitions;

a data transmitter, responsive to the mode control signal, for selectively inverting the second video data and transmitting the selectively inverted video data; and

a data receiver, responsive to the mode control signal, for selectively inverting the selectively inverted video data from the data transmitter to reconstruct the inverted video data into the second video data.

41. A computer system including a liquid crystal display device and a video card for producing video data to be supplied to the liquid crystal display device, said system comprising:

a mode controller for receiving video data having a plurality of bits from the video card to detect a number of bit transitions between a first video data and a second video data and for generating a mode control signal having a logic value changing in accordance with the number of bit transitions;

a data transmitter, responsive to the mode control signal, for selectively inverting the second video data and transmitting the selectively inverted video data; and

a data receiver, responsive to the mode control signal, for selectively inverting the selectively inverted video data inputted, via a transmission line, from the data transmitter and for reconstructing the inverted video data into the second video data.

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